28PH

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE MATTER OF:

GROUP: 2827

Jin Chuan BAI

SERIAL NO.: 09/921,150

EXAMINER: ZARNEKE, David A.

FILED: August 2, 2001

FOR: PACKAGING PROCESS FOR SEMICONDUCTOR PACKAGE

RESPONSE

Assistant Commissioner of Patents
& Trademarks
Washington, DC 20231

S I R:

This is in response to the outstanding office communication dated November 7, 2002. Any necessary fees should be deducted from Deposit Account No. 01-1944.

The Examiner continues to reject claims 1-8 under 35 USC 103(a) as being unpatentable over Ito, et al (U.S. Patent 6,333,206) in view of Urushima (JP 05-003183) and applicant's admitted prior art. The Examiner admits that the primary reference Ito, et al '206 teaches away from the present claims "in that the present claims call for a coplanar surface between flat ended bumps and the encapsulant" but notwithstanding considers this known from Urushima and alleges that it would have been obvious to one of ordinary skill in the art to combine the teaching of Urushima with Ito, et al. Applicant once again respectfully traverses this rejection.

Since the Examiner acknowledges that the reference Ito, et al '206 fails to teach conductive electrode portions having a flat end that is coplanar with the top of the first encapsulant, applicant believes that it is clear to the Examiner that the process as taught by applicant overcomes problems in the prior art teaching of Ito.

Applicant's invention is directed to a semiconductor packaging process by which first, a plurality of conductive elements (bumps) each having a flat end are formed on a chip-

mounting area of a substrate. Next, a first encapsulant is used to encapsulate the conductive bumps so that the top surface of the first encapsulant is flush with the flat ends of the conductive bumps for forming a coplanar surface by which the flat ends of the conductive bumps are exposed. The Examiner has apparently disregarded the significance of this distinction as more clearly defined in steps 3 and 4 of claim 1 in citing the reference Urushima (JP 05-003183). Admittedly, the Examiner is only working from an abstract of Urushima which may be the reason why the Urushima disclosure has been misapplied and is misunderstood. In Figure 1 of Urushima, a plurality of bumps 10 are formed at the ends of the pad electrodes 11 extending from the semiconductor substrate 4 over which a protective epoxy film 12 is applied. This is only the first step in the semiconductor device manufacturing technique shown in Urushima. Thereafter, as shown in Figure 2a, the bumps 10 are exposed and electrically connected to a plurality of protruding bumps 16 formed on the bond pads 13 of the substrate 15 leaving a gap (although not designated by a reference numeral) between the chip 4 and the substrate 15 no different from the gap formed in Ito '206 and for the same reasons. This will cause the same problems to which this invention is addressed. Stated otherwise, the teaching of Urushima is no different from the teaching of Ito as regards the problem of the subject invention and is not a teaching of how to avoid the formation of an underfill or a gap between the chip 4 and the substrate 15. If the gap in Urushima is intended to be filled using a conventional underfill process such as is taught in Ito, it will lead to voids and to a popcorn effect as has been discussed in the subject application. The gap is due to an incomplete gap-filling which is circumvented by the packaging process of the subject invention when the chip (flip chip) is mounted on the coplanar surface formed by the first encapsulant and the conductive bumps. The bond pads on the chip are electrically connected to the exposed ends of the conductive bumps. In the subject invention, a second encapsulant is formed to encapsulate the chip after the electrical connection is made. The coplanar surface arrangement of step 3 in claim 1 assures an attachment free of gaps between the chip and the first encapsulant. There is no such teaching in Urushima or any suggestion in Urushima of steps 3 and 4 of claim 1.

Stated otherwise, applicant's claim 1 defines a packaging process for a semiconductor package in which step 3 requires the first encapsulant to be formed on the chip-mounting area of the substrate for encapsulating the conductive elements so that the ends of the conductive elements are exposed to the outside of the first encapsulant with the first encapsulant

forming a common coplanar surface with the exposed ends of the conducting elements permitting the surface of the semiconductor chip to be attached to the coplanar surface without forming a gap between the semiconductor chip and the coplanar surface. This is not taught in Urushima and cannot be read into Urushima.

The arguments of the Examiner are apparently based on a misunderstanding of the teaching of the reference Urushima derived solely from the illustrated drawing of Figure 1 which is not appropriate to a rejection under 35 USC 103. If the Examiner is in disagreement with this, applicant would like to have an interview in person or on the telephone and is willing to file a Declaration under Rule 132 from the applicant regarding the actual teaching of Urushima.

For all of the above reasons, claims 1-8 are clearly patentable over the references cited of record taken individually or in combination with or without the combination of applicant's alleged admitted prior art.

Reconsideration and allowance of the subject application is respectfully solicited.

Respectfully submitted,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed: Commissioner of Patents & Trademarks, Washington, DC 20231 on February 7, 2003.

Date: Feb. 7, 2003